Form PTO-1449 U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No. BDG018	Serial No.
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant Chia-Chung Wang et al.	
	Filing Date	Group Art Unit

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
PD	AA	4,955,523	09/1990	Calomagno et al.	228	179	
	AB	4,970,571	11/1990	Yamakawa et al.	357	71	
	AC	4,984,358	01/1991	Nelson	29	830	
	AD	5,074,947	12/1991	Estes et al.	156	307.3	
	AE	5,106,461	04/1992	Volfson et al.	205	125	
	AF	5,116,463	05/1992	Lin et al.	156	653	
	AG	5,137,845	08/1992	Lochon et al.	437	183	
	AH	5,167,992	12/1992	Lin et al.	427	437	
	AI	5,196,371	03/1993	Kulesza et al.	437	183	
	AJ	5,209,817	05/1993	Ahmad et al.	156	643	
	AK	5,237,130	08/1993	Kulesza et al.	174	260	
	AL	5,260,234	11/1993	Long	437	203	
PD	AM	5,261,593	11/1993	Casson et al.	228	180.22	

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
PD	AN	EP 0 718 882 A1	06/1996	European Patent Office	H01L	23/057		
PD	AO	WO 97/38563	10/1997	WIPO	H05K	1/03		

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

PD	AP	Markstein et al., "Controlling the Variables in Stencil Printing," Electronic Packaging & Production, February 1997, pp. 48-56.
PD	AQ	Elenius, "Choosing a Flip Chip Bumping Supplier - Technology an IC Package contractor should look for," Advanced Packaging, March/April 1998, pp. 70-73.

Examiner PHUC T. DANG	Date Considered 9/28/2004

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your next communication to Applicant.

Form PTO-1449 U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No. BDG018	Serial No. 10/646,415
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant Chia-Chung Wang et al.	
	Filing Date August 22, 2003	Group Art Unit

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
PD	AA	6,137,163	10/24/00	Kim et al.	257	686	
	AB	6,180,881	01/30/01	Isaak	174	52.4	
	AC	6,188,127	02/13/01	Senba et al.	257	686	
	AD	6,235,554	05/22/01	Akram et al.	438	109	
	AE	6,335,565	01/01/02	Miyamoto et al.	257	686	
	AF	6,492,718	12/10/02	Ohmori	257	686	
PD	AG	6,564,454	05/20/03	Glenn et al.	29	852	
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AN							
	AO							

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

	AP	
	AQ	

Examiner	Date Considered
PHUC T. DANG	9/28/2004

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	Filing Date August 22, 2003	Group Art Unit

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
PP	AA	5,149,958	09/1992	Hallenbeck et al.	250	216	
	AB	5,523,608	06/1996	Kitaoka et al.	257	433	
	AC	5,834,835	11/1998	Maekawa	257	680	
	AD	5,893,723	04/1999	Yamanaka	438	65	
	AE	5,929,516	07/1999	Heerman et al.	257	701	
PP	AF	6,001,671	12/1999	Fjelstad	438	112	
	AG						
	AH						
	AI						
	AJ						
	AK						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

PP	AN	Harper, "Electronic Packaging and Interconnection Handbook," Third Edition, Published by McGraw-Hill, 2000, page 7.42.
	AM	Towle et al., "Bumpless Build-Up Layer Packaging," 7 pages, downloaded from www.Intel.com on November 1, 2002.
	AN	Towle et al., "Bumpless Build-Up Layer Packaging," 19 pages, dated November 11, 2001, downloaded from www.Intel.com on November 1, 2002.
	AO	Teixeira, "Bumpless Build-Up Layer Packaging Technology," Intel Backgrounder, 4 pages, downloaded from www.Intel.com on November 1, 2002.
	AP	Braunisch et al., "Electrical Performance of Bumpless Build-Up Layer Packaging," 15 pages, downloaded from www.Intel.com on November 1, 2002.
PD	AQ	Braunisch et al., "Electrical Performance of Bumpless Build-Up Layer Packaging," 2002 Electronic Components and Technology Conference, 6 pages, downloaded from www.Intel.com on November 1, 2002.

Examiner	Date Considered
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